ABSTRACT OF THE DISCLOSURE

A connection gate circuit includes first and second N channel MOS transistors connected in series between a first bit line of a pair of bit lines and a first global IO line of a pair of IO lines, and third and fourth N channel MOS transistors connected in series between a second bit line of the pair of bit lines and a second global IO line of the pair of IO lines. The first and second N channel MOS transistors have their gates receiving a sense amplifier activation signal activating a sense amplifier. The third and fourth N channel MOS transistors have their gates receiving a column selection signal.